In the Abstract:

~~Integrated circuit arrangement with capacitor and fabrication method~~

~~An explanation is given, inter alia, of an integrated circuit arrangement (120), which contains a transistor (122), preferably a so-called FinFET, and a capacitor (124). The bottom electrode of the capacitor (124) is arranged together with a channel region of the transistor (122) in an SOI substrate. The circuit arrangement (120) is simple to fabricate and has outstanding electronic properties.~~

~~(figure 17)~~

An integrated circuit arrangement contains an insulating region, which is part of a planar insulating layer, and a capacitor which contains: near and far electrode regions near and remote from the insulating region and a dielectric region. The capacitor and an active component are on the same side of the insulating layer, and the near electrode region and an active region of the component are planar and parallel to the insulating layer. The near electrode region is monocrystalline and contains multiple webs. Alternately, a FET is present in which: a channel region is the active region, the FET contains a web with opposing control electrodes connected by a connecting region that is isolated from the channel region by a thick insulating region. The thick insulating region is thicker than control electrode insulation regions. The control electrodes contain the same material as the far electrode region.